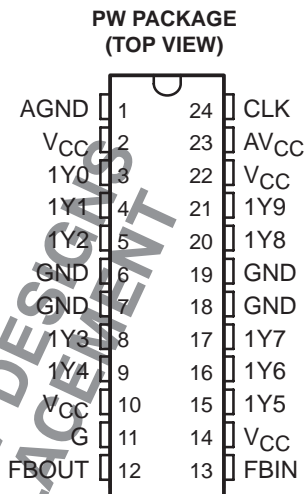


# CDC2510

## 3.3-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS597B – DECEMBER 1997 – REVISED DECEMBER 2004

- Use **CDCVF2510A** as a Replacement for this Device
- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes One Clock Input to One Bank of Ten Outputs
- Single Output Enable Terminal Controls All Ten Outputs
- External Feedback (FBIN) Pin Is Used to Synchronize the Outputs to the Clock Input
- On-Chip Series Damping Resistors
- No External RC Network Required
- Operates at 3.3-V  $V_{CC}$
- Packaged in Plastic 24-Pin Thin Shrink Small-Outline Package



### description

The CDC2510 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC2510 operates at 3.3-V  $V_{CC}$  and provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of ten outputs provide ten low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. All outputs can be enabled or disabled via a single output enable input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDC2510 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2510 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping  $AV_{CC}$  to ground.

The CDC2510 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

INPUTS		OUTPUTS	
G	CLK	1Y (0:9)	FBOUT
X	L	L	L
L	H	L	H
H	H	H	H



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PRODUCTION DATA** information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

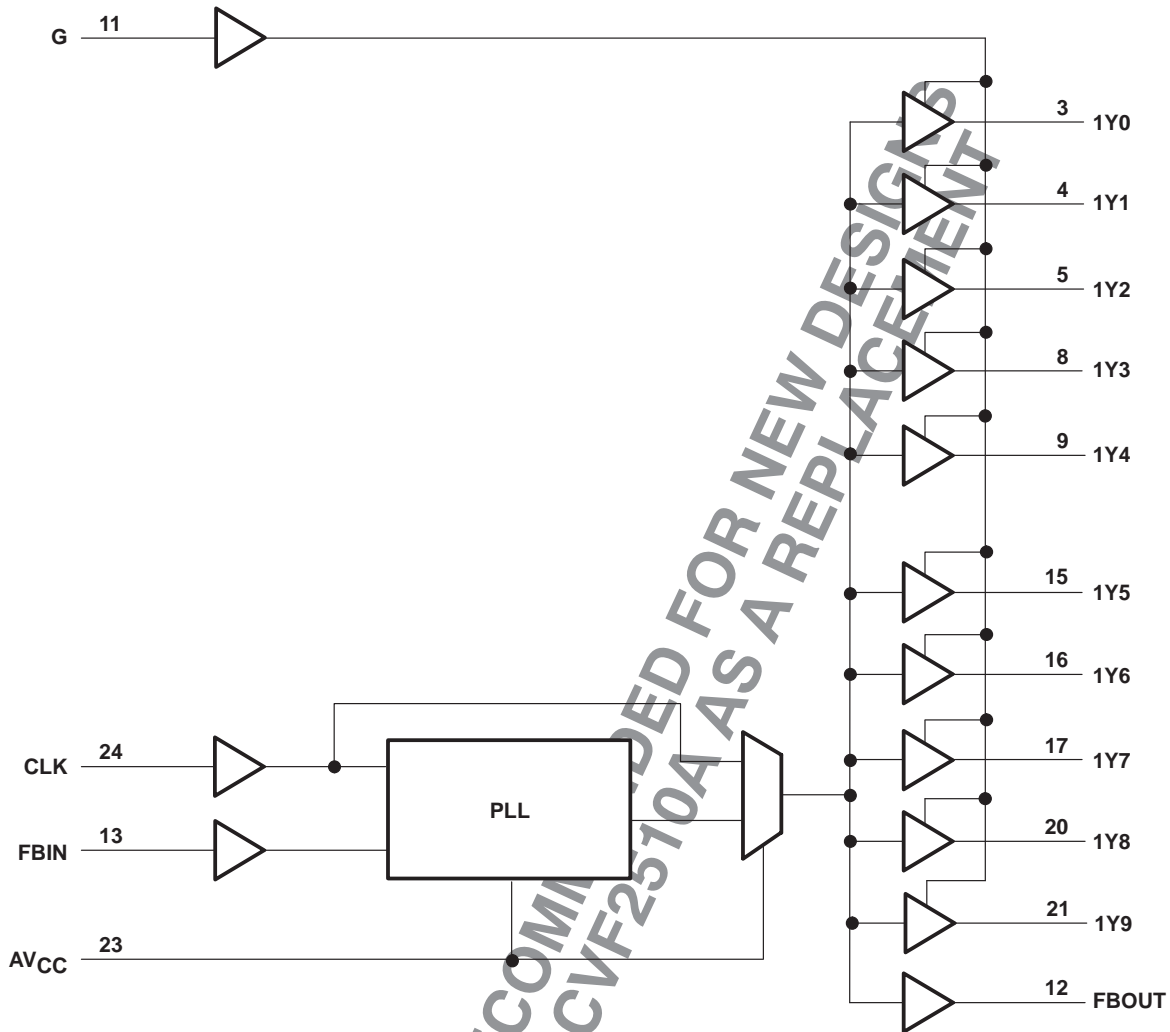
Copyright © 2004, Texas Instruments Incorporated

# CDC2510

## 3.3-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS597B – DECEMBER 1997 – REVISED DECEMBER 2004

### functional block diagram



#### AVAILABLE OPTIONS

TA	PACKAGE
	SMALL OUTLINE (PW)
0°C to 70°C	CDC2510PWR

# CDC2510

## 3.3-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS597B – DECEMBER 1997 – REVISED DECEMBER 2004

### Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDC2510 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
G	11	I	Output bank enable. G is the output enable for outputs 1Y(0:9). When G is low, outputs 1Y(0:9) are disabled to a logic-low state. When G is high, all outputs 1Y(0:9) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25- $\Omega$ series-damping resistor.
1Y(0:9)	3, 4, 5, 8, 9 15, 16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:9) is enabled via the G input. These outputs can be disabled to a logic-low state by deasserting the G control input. Each output has an integrated 25- $\Omega$ series-damping resistor.
AV <sub>CC</sub>	23	Power	Analog power supply. AV <sub>CC</sub> provides the power reference for the analog circuitry. In addition, AV <sub>CC</sub> can be used to bypass the PLL for test purposes. When AV <sub>CC</sub> is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V <sub>CC</sub>	2, 10, 14, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

NOT RECOMMENDED FOR NEW DESIGNS  
USE CDCVCF2510A AS REPLACEMENT

# CDC2510

## 3.3-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS597B – DECEMBER 1997 – REVISED DECEMBER 2004

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3)	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This value is limited to 4.6 V maximum.
  3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

### recommended operating conditions (see Note 4)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	3	3.6	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–12	mA
$I_{OL}$ Low-level output current		12	mA
$T_A$ Operating free-air temperature	0	70	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{IK}$	$I_I = -18$ mA	3 V			–1.2	V
$V_{OH}$	$I_{OH} = -100$ $\mu$ A	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -12$ mA	3 V	2.1			
	$I_{OH} = -6$ mA	3 V	2.4			
$V_{OL}$	$I_{OL} = 100$ $\mu$ A	MIN to MAX			0.2	V
	$I_{OL} = 12$ mA	3 V			0.8	
	$I_{OL} = 6$ mA	3 V			0.55	
$I_I$	$V_I = V_{CC}$ or GND	3.6 V			±5	$\mu$ A
$I_{CC}^{\S}$	$V_I = V_{CC}$ or GND, $I_O = 0$ , Outputs: low or high	3.6 V			10	$\mu$ A
$\Delta I_{CC}$	One input at $V_{CC} - 0.6$ V, Other inputs at $V_{CC}$ or GND	3.3 V to 3.6 V			500	$\mu$ A
$C_i$	$V_I = V_{CC}$ or GND	3.3 V		4		pF
$C_o$	$V_O = V_{CC}$ or GND	3.3 V		6		pF

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>§</sup> For  $I_{CC}$  of  $AV_{CC}$ , see Figure 5.



# CDC2510

## 3.3-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS597B – DECEMBER 1997 – REVISED DECEMBER 2004

### timing requirements over recommended ranges of supply voltage and operating free-air temperature

	MIN	MAX	UNIT
$f_{\text{clock}}$ Clock frequency	25	125	MHz
Input clock duty cycle	40%	60%	
Stabilization time <sup>†</sup>		1	ms

<sup>†</sup> Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 30$ pF (see Note 5 and Figures 1 and 2)<sup>‡</sup>

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.165 \text{ V}$			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{\text{phase error reference}}$ (see Figure 3)	66 MHz < CLKIN $\uparrow$ < 100 MHz	FBIN $\uparrow$				-0.7...0.1			ns
$t_{\text{phase error - jitter}}$ (see Note 6)	CLKIN $\uparrow$ = 100 MHz	FBIN $\uparrow$	-500		-50	-310			ps
$t_{\text{sk}(o)}$ <sup>§</sup>	Any Y or FBOUT	Any Y or FBOUT						200	ps
Jitter(pk-pk)	F(clkin > 66 MHz)	Any Y or FBOUT				-100		100	ps
Duty cycle reference (see Figure 4)		Any Y or FBOUT				43%		55%	
$t_r$		Any Y or FBOUT		1.3	1.9	0.8		2.1	ns
$t_f$		Any Y or FBOUT		1.7	2.3	1.2		2.5	ns

<sup>‡</sup> These parameters are not production tested.

<sup>§</sup> The  $t_{\text{sk}(o)}$  specification is only valid for equal loading of all outputs.

NOTES: 5. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

6. Phase error does not include jitter. The total phase error is -600 ps to 50 ps for the 5%  $V_{CC}$  range.

NOT RECOMMENDED FOR NEW DESIGNS  
USE CDC2510 AS A REPLACEMENT

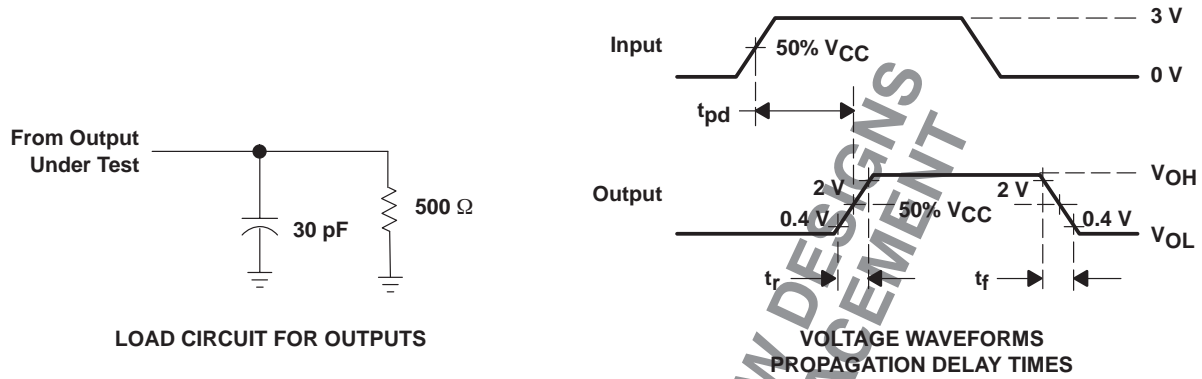


# CDC2510

## 3.3-V PHASE-LOCK LOOP CLOCK DRIVER

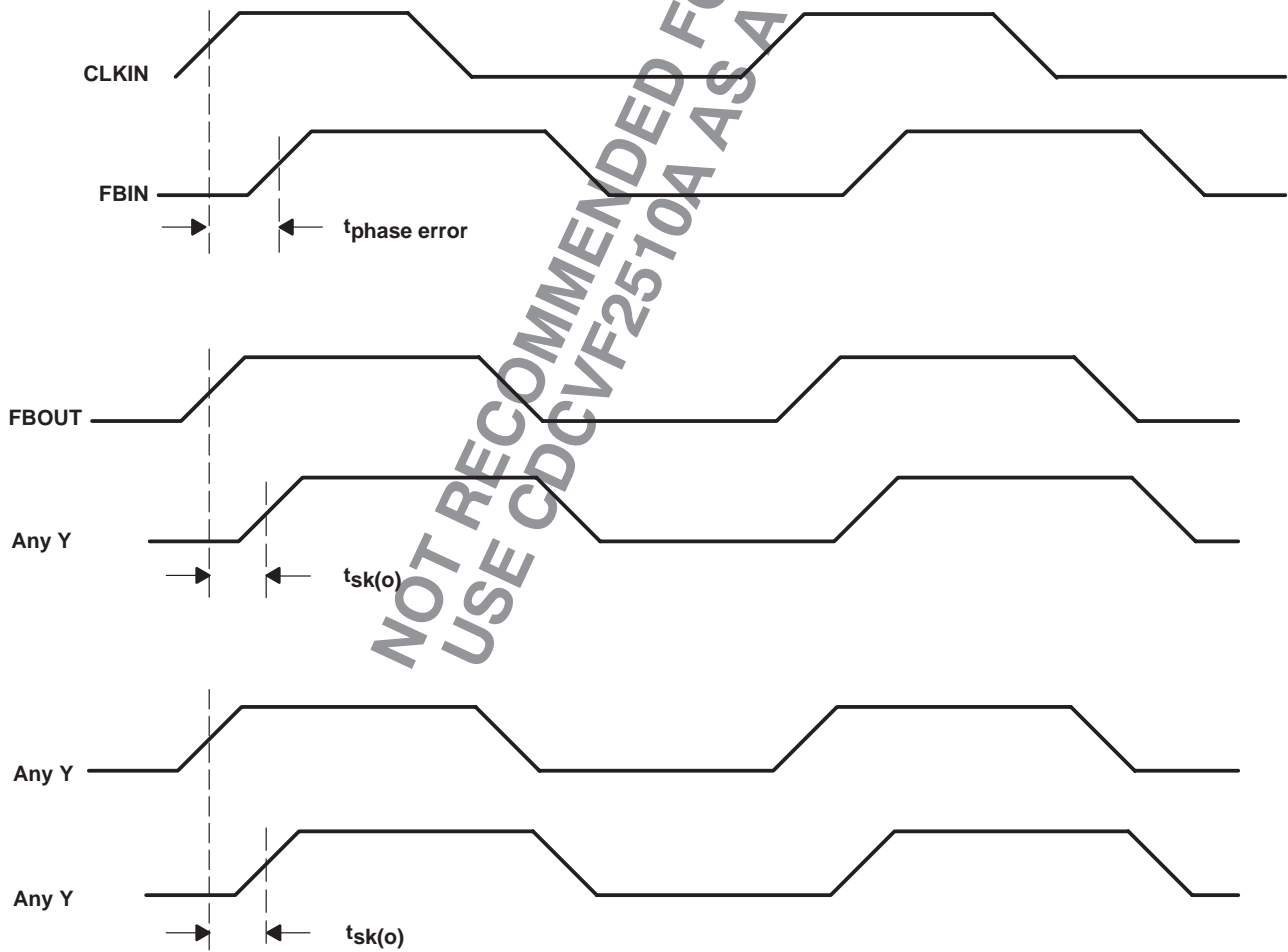
SCAS597B – DECEMBER 1997 – REVISED DECEMBER 2004

### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 100$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 1.2$  ns,  $t_f \leq 1.2$  ns.
  - C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



TYPICAL CHARACTERISTICS

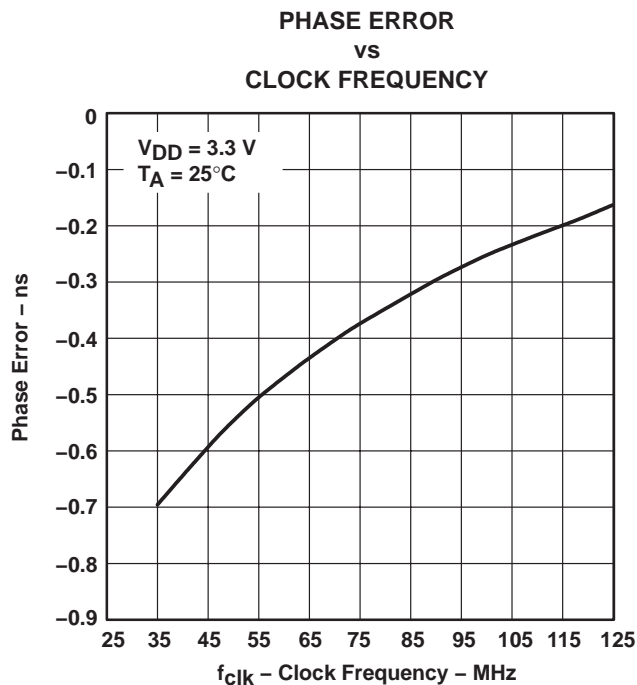


Figure 3

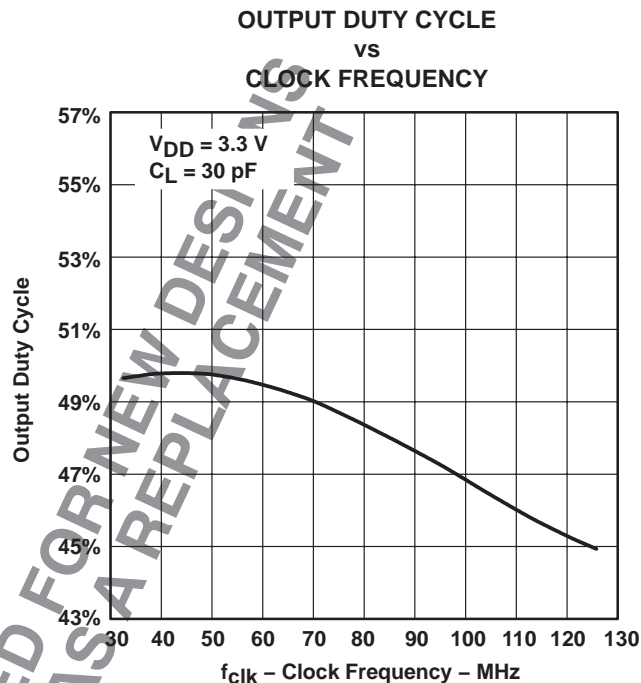


Figure 4

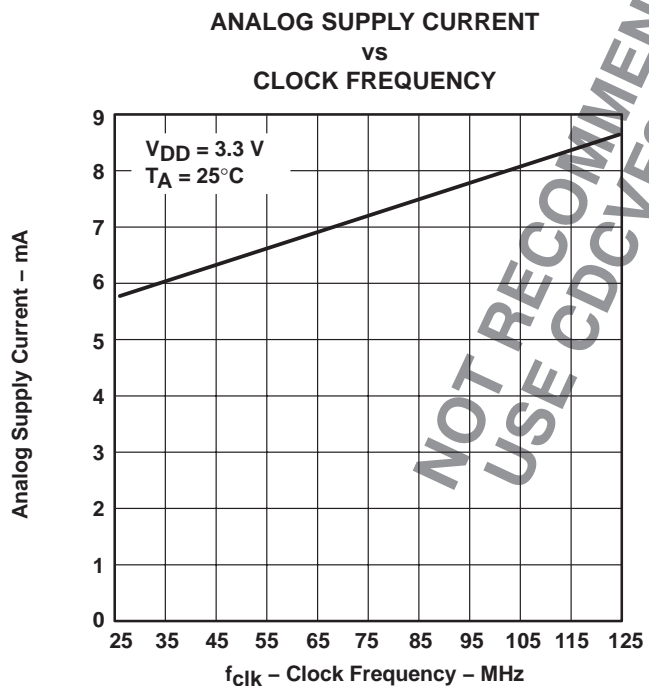


Figure 5

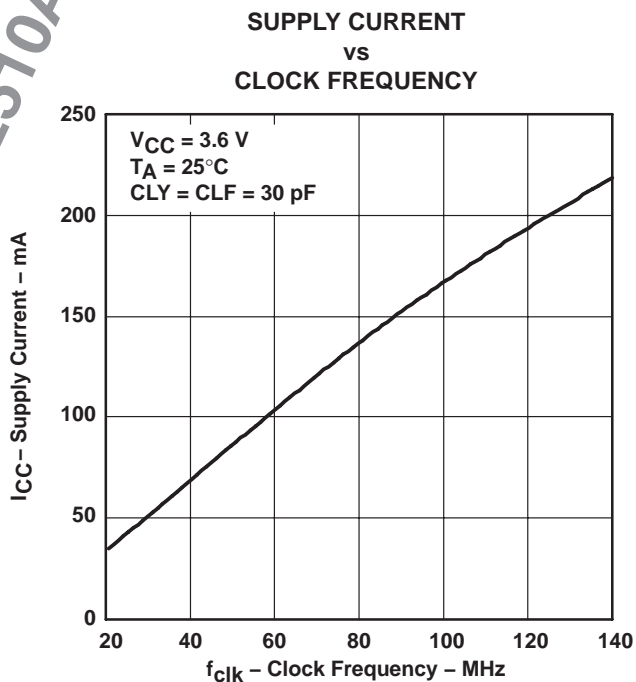


Figure 6

# CDC2510

## 3.3-V PHASE-LOCK LOOP CLOCK DRIVER

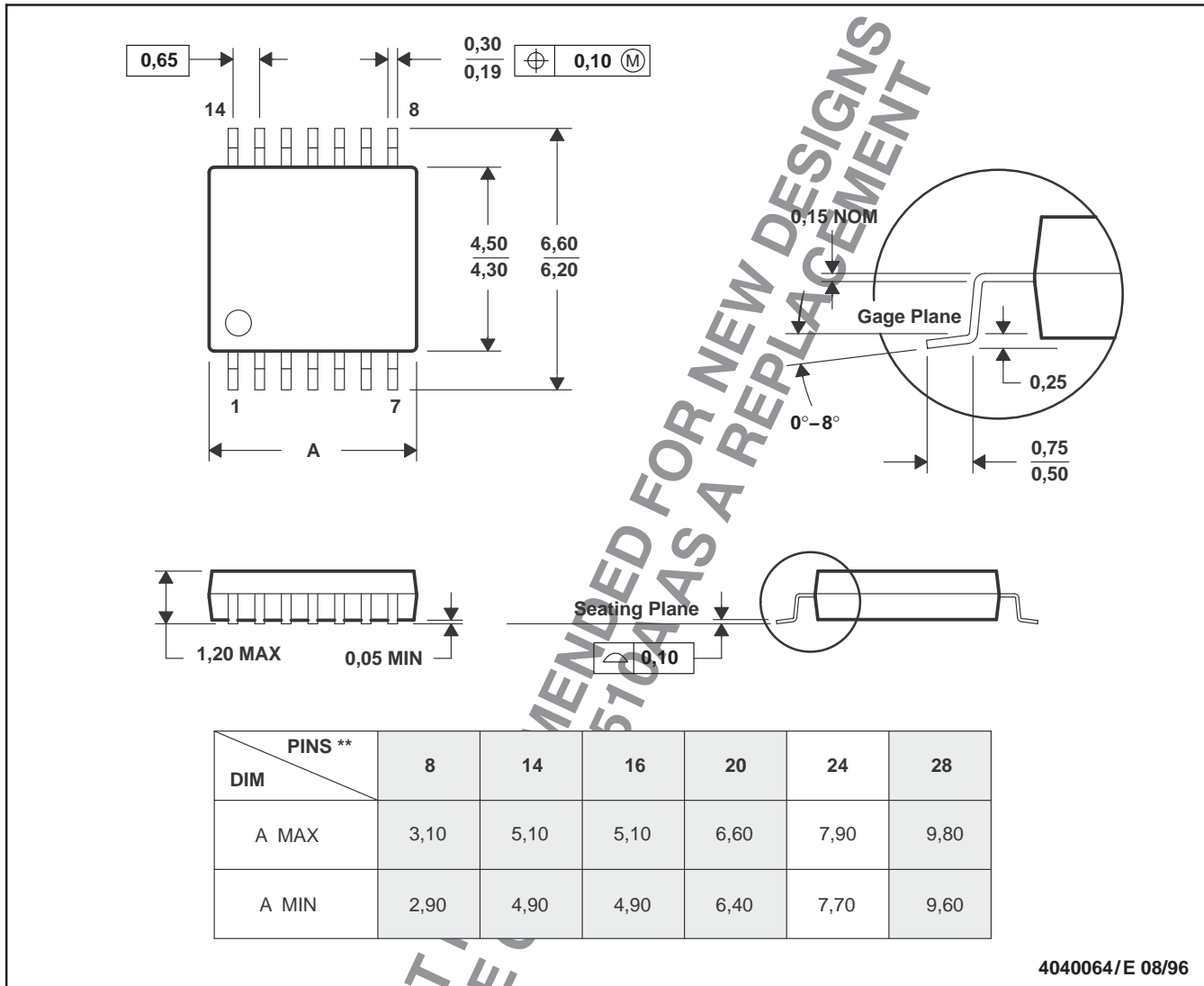
SCAS597B – DECEMBER 1997 – REVISED DECEMBER 2004

### MECHANICAL INFORMATION

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



4040064/E 08/96

- NOTES: D. All linear dimensions are in millimeters.  
 E. This drawing is subject to change without notice.  
 F. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 G. Falls within JEDEC MO-153



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDC2510PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CDC2510PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC2510PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC2510PWR	TSSOP	PW	24	2000	346.0	346.0	33.0

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2008, Texas Instruments Incorporated